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ABSTRACT

2 A transistor structure having a dedicated erase gate where the transistor can be used as a
3 memory cell is disclosed. The presently preferred embodiment of the transistor comprises a
4 floating gate disposed on a substrate and having a control gate and an erase gate overlapping said
5 floating gate, with drain and source regions doped on the substrate. By providing a dedicated
6 erase gate, the gate oxide underneath the control gate can be made thinner and can have a
7 thickness that is conducive to the scaling of the transistor. The overall cell size of the transistor
8 remains the same and the program and read operation can remain the same. Both the common
9 source and buried bitline architecture can be used, namely twin well or triple well architectures.
10 A memory circuit using the transistors of the present invention is disclosed as well for flash
11 memory circuit applications.

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